(10) Patent No.: (45) Date of Patent: ... ... Patent **States Patent** United Landau (12)

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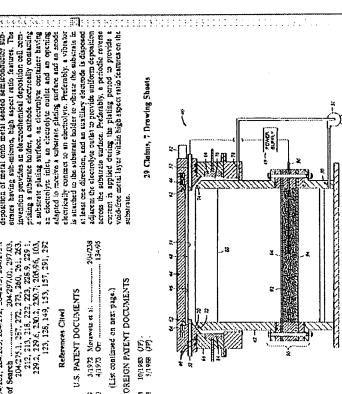
Primary Examinar—Bruce F. Bell (74) Anorney, Agent, or Firm—Thomason, Paterson, L.L.P.

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ABSTRACT

deposition of metal onto metal seeded semiconductor sub-strate having sub-mixton, blag aspect and for features. The invention provides an electrochemical deposition cell com-prising a substrate holder, a cathode electrocally contacting a substrate plaing surface, an electrolyte continuer having an electrolyte infett, an electrolyte continuer having and electrolyte infett, an operation adapted to more and an operation achieving reliable, consistent meral electroplating or elec-trochemical deposition onto semiconductor substrates. More raciculariy, the invention provides uniform and void-free The invention provides an apparatus and 2/54/238



Laventor: Undel Landau, Cleveland, OH (US) ELECTRO-CHEMICAL DEPOSITION SYSTEM AND METHOD OF ELECTROPLATING ON SUBSTRATES £ 3

Applied Materials, Inc., Santa Clara, CA (US) Assignee Notice:

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Subject to any disclaimer, the term of this parm is extended or adjusted under 35 parent is extended or adjusted under U.S.C. 154(b) by 0 days.

Appl. No.: 09/205,678 <u>5</u> Apr. 21, 1999 Filed

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Related U.S. Application Data Provisions! application No. 60:03.2513, the6 on Apr. 23, 1998. <u>ફ</u>

U.S. CI. 2065/16 2065/05 2055/105 2057/25 2065/26 2065/105 2057/25 2067/26 2067/26 2067/26 2067/26 2067/26 2067/26 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 2067/27 206 C25D 5/00 In C (25)

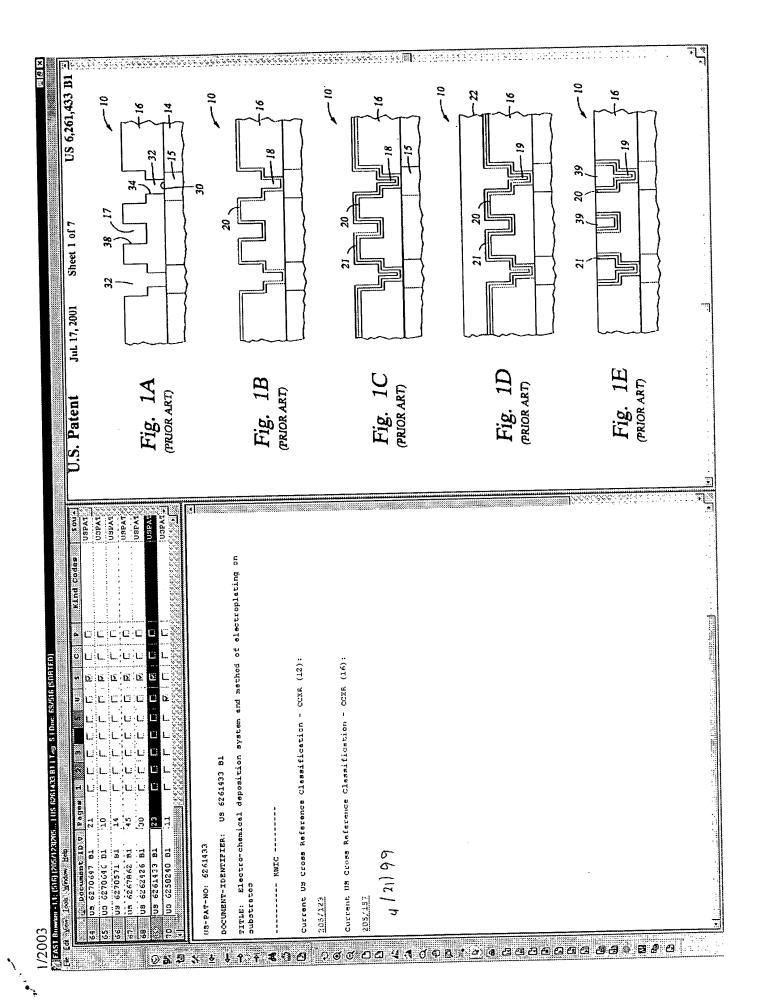
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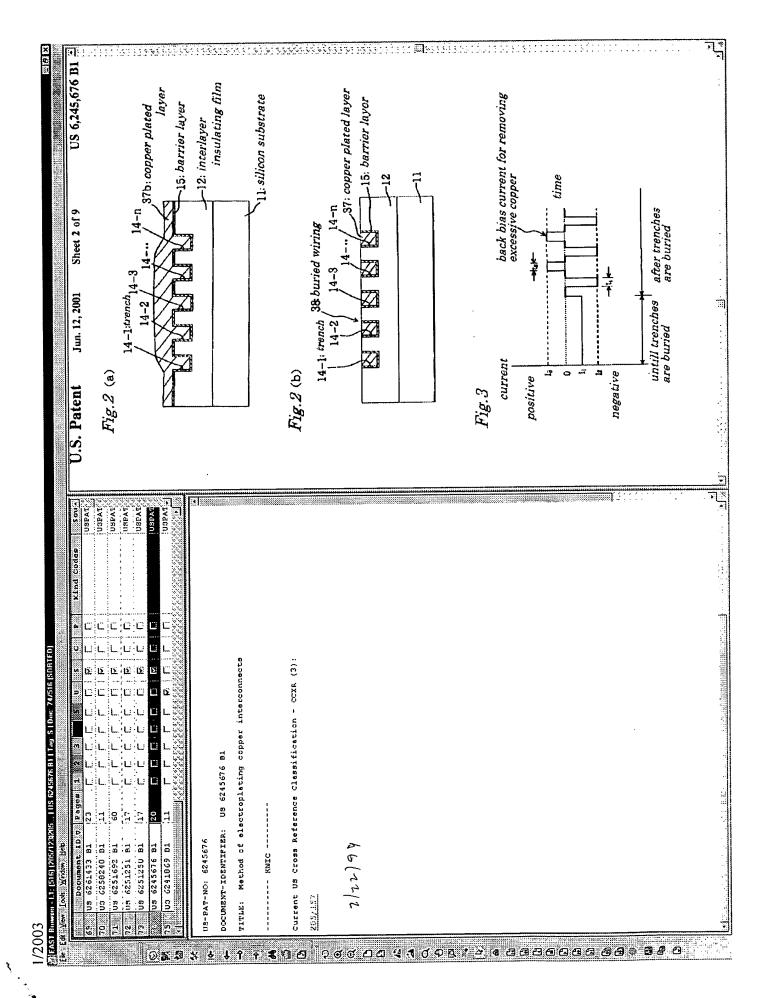
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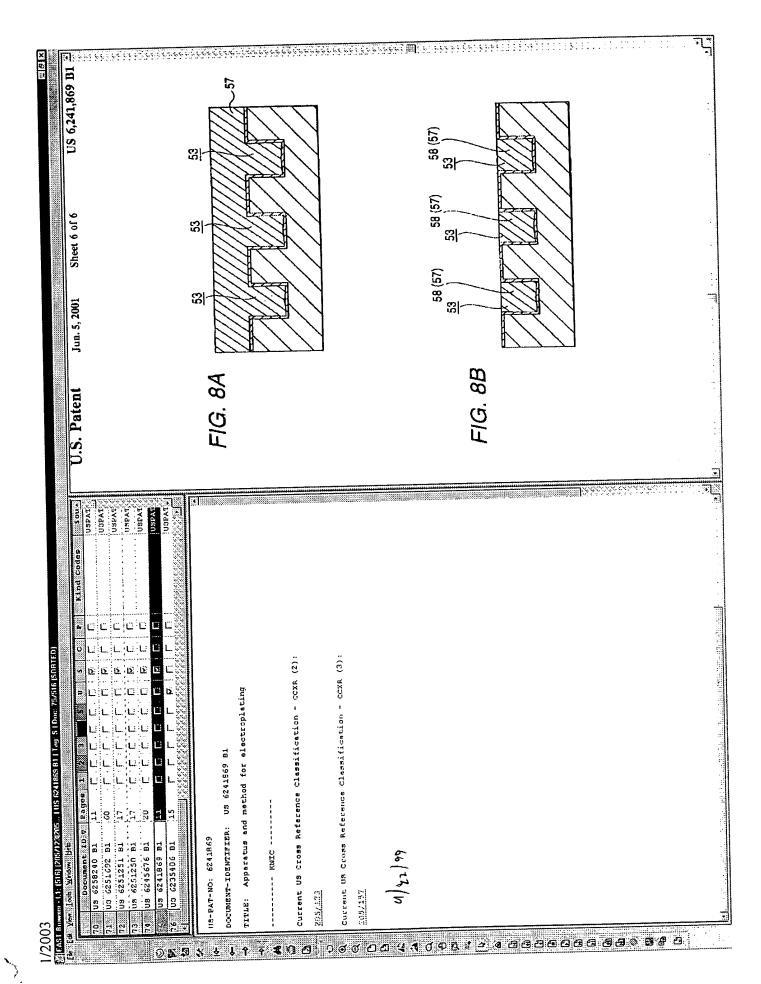


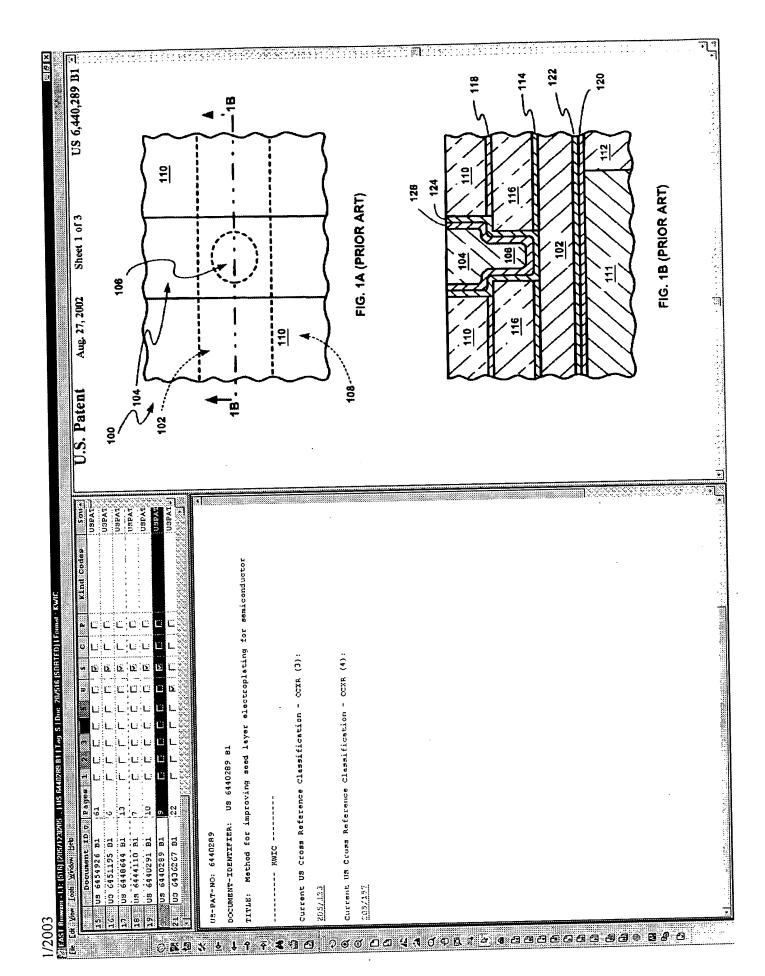
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× 8 % An apparatus and a method for electroplating for forming a meral film by an electroplating method. The apparatus comprises a plating bath provided in a non-oxidative amosphere, and in the method, at article to be plated is amosphere, and in the method, at article to be plated in primersed in 2 plating bath through a non-oxidative atmosphere. 257/762 Printry Examiter—Edta Vicing (74) Attorney, Agent, or Firm—Ronald P. Kananen; Rader, Fishman & Grave: Jun. 5, 2001 US 6,241,869 B1 757 FOREIGN PATENT DOCUMENTS U.S. PATENT DOCUMENTS 7 Claims, 6 Drawing Shoets References Cited 5,273,642 \* 12,1993 Offes et al. 5,763,953 \* 6,1998 fijms et al. ARSTRACT (10) Patent No.: (45) Date of Patent: 4-131395 \* 5/1992 (JP) 53 cited by examiner 56 98 53 C250 547 C250 702; C250 548 C250 548 C250 548 C250 547 205137; 205137; 205138; 205138 205137; 205, 224, 115, 124, 427,946; 205,137 Subject to any disclaimer, the torm of this pasen is extended or adjusted urder 35 U.S.C. 154(b) by 0 days. 10-114494 inventor: Keffehl Masch, Kanagawa (JP) Sony Corporation, Thkyo (JP) **States Patent** Foreign Application Priority Date APPARATUS AND METHOD FOR ELECTROPLATING Apr. 22, 1999 53 Appl. No.: 09/296,297 Field of Search £ (12) United 56 Assignee: U.S. Cl. (S1) Int. CL.7 Maeda Notice: Apr. 24, 1998 Filed: (B) (25) 38 (3) 9 (34) 8 3 USPAT USPAT USPAT USPAT USPAT USPAT USPAT Kind Ü u Ü | | FAST Browser - L1; [516] [205/123/205. . 1115 6241869 B1 | Tay. S | Doc. 75/516 [SDRTED] 3 3 [2] CCXR SCXB Ш method for electroplating Ü Reference Classification Classification . U Ü D US 6241869 L D ען ען ען ע Reference <sub>७</sub>ान Ξ r Apperatus and DOCUMENT-IDENTIFIER: US 6235406 B1 113-PAT-NO: 6241869 퉑 US 6228293 BI us 6245676 B1 us 6241869 D1 US 6224737 B1 US 6224735 B1 Cross Cross KNIC Lock Mendow 5 5 Current Current 305/197 557.123 TITLE: > 0 0 0 0 0 4 1 0 0 8 1 2 0 5 5 5 6 6 6 8 8 8 0 **8 9** X ↓ ተ <del>፣</del> **4**90

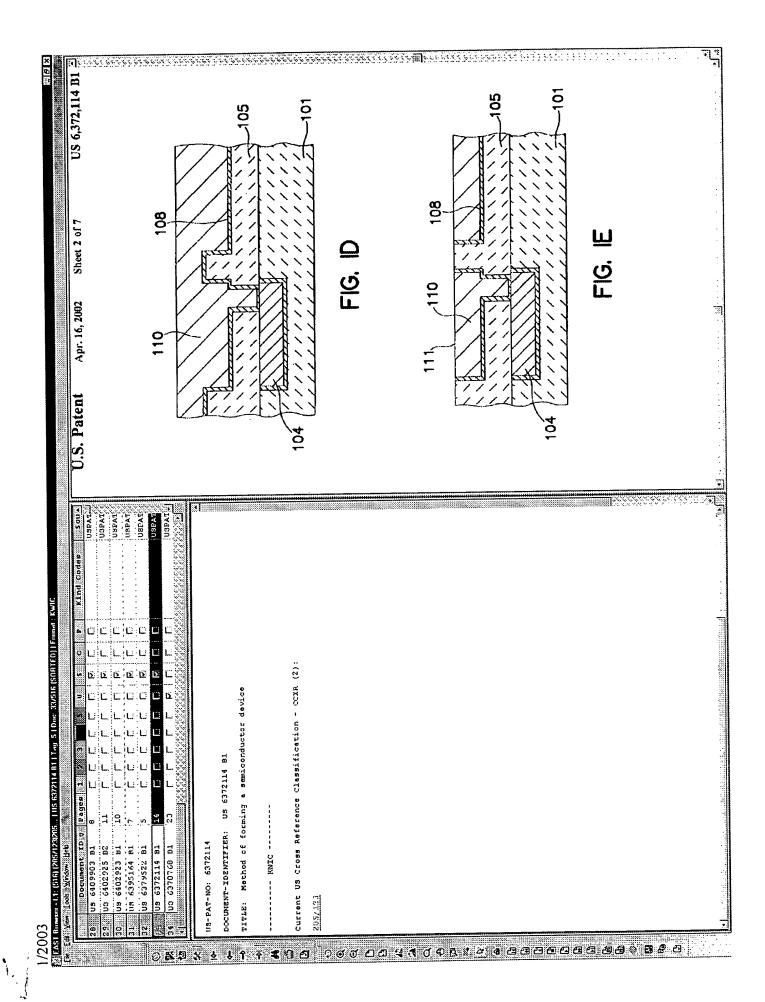




leting layer comprises the steps of selectively depositing a harrier layer on a predetermined region of an insulating layer by use of a first deposition mask; selectively depositing a mutal seed layer made of a metal which is different in exclasse from the barrier layer by use of a second deposition mask, so that the metal seed layer extands not only on an entire surface of the barrier layer but is size a peripheral. ≈ 8 × region positioned outside the predetermined region of the insulating layer and forming a metal plating tayer made of the metal of the metal seed layer, so that the metal plating layer is athered on the metal seed layer, whereby the metal plating layer is separated from the beautiful to be arrived to the metal from the insulating layer is separated from the barrier layer and also from the insulating layer. A method of forming a multi-layer structure over an insu-Apr. 16, 2002 6/1991 ...... HOLL/20205 Scloway. US 6,372,114 B1 Prinary Examiner—Rodiney G. McDonald (74) Automers; Agent, or Firm—Hayes, Hemessey, Grossman & Hage, P.C. FOREIGN PATENT DOCUMENTS 6 Clulus, 7 Drawing Sheets References Cited ABSTRACT (10) Patent No.: (45) Date of Patent: 3-145826 0 જુ e; 60 9 Subject to any disclaimer, the term of this parent is extended or adjusted under 35 U.S.C. 154(b) by 0 days. .. 10-095502 108 Assignee: NEC Corporation, Tokyo (JP) Foreign Application Priority Date (12) United States Patent lavestor: Nobukaru Ito, Tokye (JP) METHOD OF FORMING A SEMICONDUCTOR DEVICE Apr. 8, 1999 Appl. No.: 09/288,265 6 (51) Int. Ct.7 Apr. 8, 1998 Notice: Filed Ito (22) (38) <u>(5</u> 33 99 Ê 0 ₹ 6 USPAT USPAT USPAT USPAT USPAT USPAT USPAT ejejeje c c تاليا wsei - 1.1; (516) (205/12/32/05... 111S 6372114 811 Tay S 1 Dire: 33/516 (SNRTED) Gross Reference Classification - GCXR (2): D D D D  $\Sigma$ 12 ĺΣ Method of forming a semiconductor device C L. US 6372114 B1 u-u Document ID 0 Rages 1 82 23 74 59 DOCUMENT-IDENTIFIER: US-PAT-NO: 6372114 US 6350364 B1 US 6379522 BI US 6372114 BI 118 6370768 BL us 6361675 Bi US 6358388 B1 US 6395164 B1 23 See See Current 2657.103 TITLE: MEAST Bu ରିଅଷ୍ଟ ନ୍ଶ୍ର କ୍ୟାସ ଓର୍ଡ ପସ ଶସ ପ୍ରସ୍<u>ତ, ବ୍ରଳ୍ପତ</u> ଅପେତ ଅପେତ । 80

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hyer baving an upper surface and a predetermined fishkness is electrolytically deposited over the first copper containing layer. The second expert deposition step has a second rain of trigilateness concentration that is less than he said first ratio of brightness concentration that is hest than he said first ratio of brightness concentrationshes, else a concentration. The second copper containing layer upper surface thanks a greater planathy than the first copper containing layer upper surface of the copper containing layer upper surface of the circumstance of levelers telesive to the brightness in the election byte bath. the section of the se × 9 🕾 copper containing layer having an upper surface and a predetermined thickness within the trench. The first copper 205/184 257/762 205/101 205/116 205/116 A method for electroplating copper in trenches, including the steps of providing a semiconductor substrate baving a trench formed therein and electrolytically depositing a first Prinary Examinar—Kathya Gorgos Assistan Examina—Eises Soith-Hiska (74) Artornoy, Agont, or Firm—George O. Sailes, Stephen B. Askermen, Stephen G. Staaton deposition step has a first ratio of brighteners concentration-Feb. 26, 2002 6,350,364 B1 Nogani et el.

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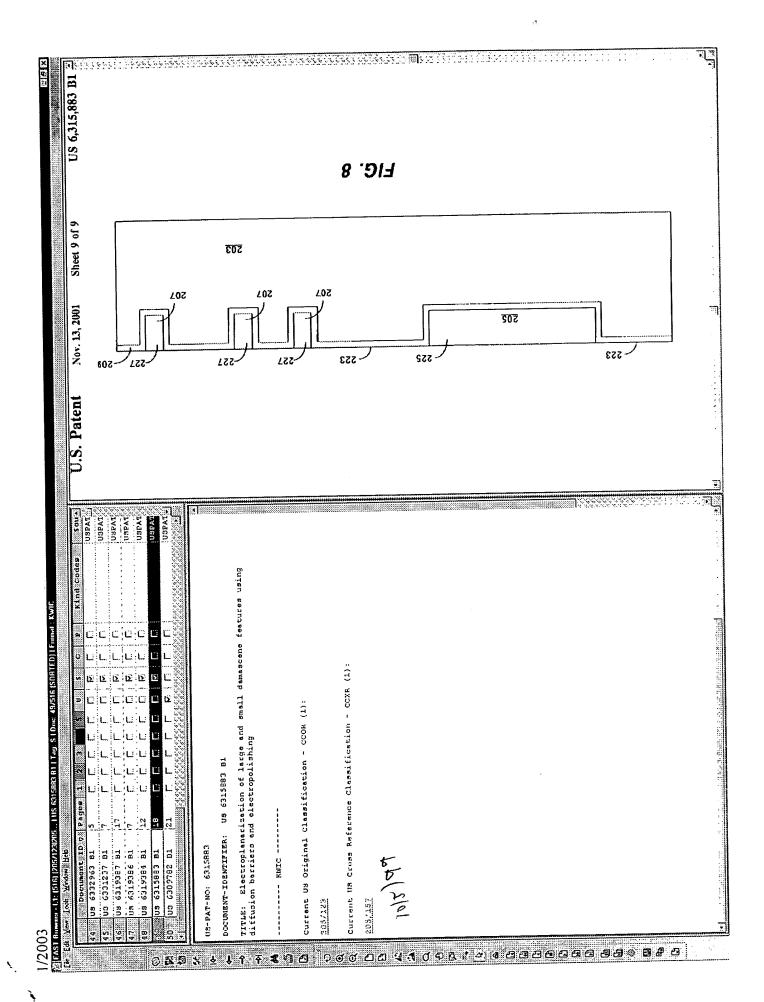
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That et al. 0 20 Claims, 1 Drawing Sheet S ABSTRACT 5,566,333 A - 10,1959 N 5,000,422 A - 10,1959 II 5,012,192 A - 10,1959 D 6,108,704 B1 - 5,700, IN (10) Patent No.: (45) Date of Patent: 8 2 cited by exeminer ω (3) ... 205/118; 205/157; 205/170; 205/182 205/118, 157, 205/170, 182 205/122 437/195 205/122 437/238 205/87 433/678 433/678 C25D 5/02; C25D 7/12; C25D 5/10 Subject to any disclaimer, the term of this parm is extended or adjusted under 35 U.S.C. 134(b) by 0 days. METHOD FOR IMPROVEMENT OF PLANARITY OF ELECTROPLATED COPPER Talwan Semiconductor Manufacturing Company, Hain-Chu laventor: Syun-Ming Jang, Hsia-Chu (TW) States Patent U.S. PATENT DOCUMENTS References Cited 8 Feb. 18, 2000 Appl. No.: 69/506,931 N E Field of Search 5,055,425 A 5,055,425 A 5,071,518 A 5,060,565 A 5,660,768 A 5,600,400 A United Assignee: US C Int. Cl. Notice: Filod Jang (31) (52) (58) 3 (\$5) £ 0 3 8 (23) 8 USBATE USPAT USPAT USPAT USPAT USPAT Method for improvement of planarity of electroplated capper FAST Russen - L1: (516) (2057/239265... L11S 6350364 BT LTeg. S.L.Duc. 327516 (SORTED) | Furnet: KWIC. cicc Cross Reference Classification - CCXR (1): ı. US 6350364 B1 Ш οτι 88 9 2 1.4 23 DOCUMENT-IDENTIFIER: US 6370768 BI 6350364 US 6358338 BI US 6350364 B1 ua 6350363 B1 118 6361675 BI US 6379522 5 118-PAT-NO: # 5 Current 205/153 TITLE: E.K. /2003 අුද් 9 ව වලර උප දිය් රඳදියි <u>එම ෙස විසි</u>වි ነ ይ ይሰ

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A disclose detectroplanulization process tryobys "musking" certain regions of a wrater surface during electropolishing. The regions chosen lor musking are features of relatively the regions chosen lor musking are features of relatively by specific features that are wider than they are deep). The musking is accomplished with a uniterial of relatively tow yout conductivity within differently always on relatively tow work armapor of the metal time produced during electropolishing. Examples of musking meterials helude concentrated phosphoric acid and certain polymers. H. Maria Maria Maria × 8 ≈ Prinary Examiner—Dould R. Khleadin (74) anonney, Agent, or fifmi—Beyer Weaver & Thomas (LP ã **→** 8 437,228 6,315,883 B1 Nav. 13, 2001 32 Clutms, 9 Drawing Sheets S ABSTRACT 3 (10) Patent No.: (45) Date of Patent: cited by examine Soffed. (53) C28D 5/02; C25D 5/48; C25D 7/12; C25F 3/10 C25D 7/12; C25F 3/10 C25D 7/12; C25F 3/10 C 204/129.1 Reland U.S. Application Data Provisional application No. 66/105.733, filed on Oct. 26, 1976 Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days. ELECTROPLANARIZATION OF LARGE AND SMALL DAMASCENE FEATURES USING DIFFUSION BARRIERS AND ELECTROPOLISHING Inventors: Steven T. Mayer, Robert J. Contullat. both of Lake Oswego, OR (US) Novelius Systems, Inc., San Jose, CA (US) United States Patent U.S. PATENT DOCUMENTS References Cited 3 11,1974 Talengi et al. Oct. 3, 1999 Appl. No.: 09/412,837 Field of Search Mayer et al. E. C.' 3,649,270 Assignee: U.S. CI. Notice: Filed: `.;; (25) (58) (25) (36) (§  $\hat{\mathbb{S}}$ 3 3 £ (32) E (17) USPAT USPAT USPAT USPAT USPAT USPAT USPAT TITLE: Electroplanatization of large and small damascene features using diffusion berriers and electropolishing ではないないない。 CCCC Current US Gross Reference Classification - CCXR (1): Σ  $\Sigma$ С Current Us Original Classification - CCOR Ľ Ü US 6315883 C 21 24 24 9 4 DOCUMENT-IDENTIFIER: Us 6309528 B1 Us 6300244 B1 US-PAT-NO: 6315883 17 B1 US 6299753 B1 KNIC US 6299751 US 6309782 Edit View Look Mindow 267/502 205/123 1/2003 



Spainter the facilities by the control of the contr Accessor in the second conservation of the second conservation of light having a vis-strid on a semiconductor substrate, the vis-stud being formed in a vis-toke through a burner layer formed of on throughts compound tayer or a light melting point moral layer formed on an inner sulface of the vis-solutible vis-stud being made of the same mental as a motal. forming agent, immersing the treated substrate into an electrotese plating solution, bringing a member made of the same ment is a next of formed by the electrotess plating in corpare with the electrotese plating solution, and electrically commercing the member to the barrier layer to perform compressing the barrier layer. The armiconductor device cur-be obtained by Carring the barrier layer on the intert suffree of the vis-bole in the semiconductor substrate, then treating the substrate with a treatment solution occuration a complex When a writing conductor is formed on a semiconductor substrate, a via-hole or a trench is formed by directly performing electroless plaining on a barrier layer containing a very small depriessed pertion such as the via-totic or the crackin is an insulator layer without using a dry metallized method or a substitutive plaining method. Shacham-Diamand et al. "High spect ratio quanter-micron electroles copper integrated schnology", Mucrisis for Advances Metalization, MAM 1997, pp. 11-14." Terry, Smul & insulator US 6,300,244 B1 Oct. 9, 2001 The semiconductor device is provided with an 18 Claims, 8 Drawing Shorts Primary Examinar—Charles Bower Assistant Examinar—Thathis Tham (74) Attorney, Agent, or Pirm—Attoralli, Kaus, LLP OTHER PUBLICATIONS ARSTRACT (10) Patent No.: (45) Date of Patent: 66 8 3/1996 · clied by exeminer electroless plating. 8-83796 6 23/48 437/190 265/123 437/290 438/992 438/987 Pield of Senrth 62, 438,658, 403, 438,678, 403, 438,688, 687, 675, 627, 625, 629, 427,97, 36, 438,1, 437, 304, 305, 205,473, 489, 492, 496, 499, 430, 205,133, 125, 126 Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days. Int. C1. HUIL 21/24; HUIL 21/24/63; BGD 57/2; BGD 57/2; C25. BGD 57/2; BGD 5 ..... 10-143133 SEMICONDICTOR DEVICE AND METHOD OF MANUFACTURING THE SAME invectors: Takevuki Itabashi; Toshio Haba; Haruo Akabushi, ali of Hischi (JP) TI ( ) ( ) ( ) ( ) FOREIGN PATENT DOCUMENTS Foreign Application Priority Data (12) United States Patent U.S. PATENT DOCUMENTS Assignee: Hitachi, Ltd., Tokyo (IP) References Cited May 25, 1999 (EP) Appl. No.: 09/317,955 Itabashi et al S Ń 25, 1998 (51) Int. Cl. 692554 Norice: Filed May (23) 3 (55) 3 (22) (30) 3 € £ 6 <del>ا</del> آ U3PAT USPAT USPAT USPAT USPAT Kind Codes Semiconductor device and method of manufecturing the same ceec LUUL Reference Classification - CCXR (3):  $\Sigma$ D D D B US 6300244 C 19 Έ. . DOCUMENT-IDENTIFIER: US 6299753 B1 US 6299751 B1 iis 6297157 B1 B :1 US 6300244 B1 US 6287443 B1 Cross KWIC us 6296753 US 6204121 5 UB-PAT-NO: Current 2057.123 TITLE: ිවුල් ගැන යුතු රැබුල් නැති සෙම සෙලලාලාලා ලාලා ලාලා ලාලා **≰**11 ∆

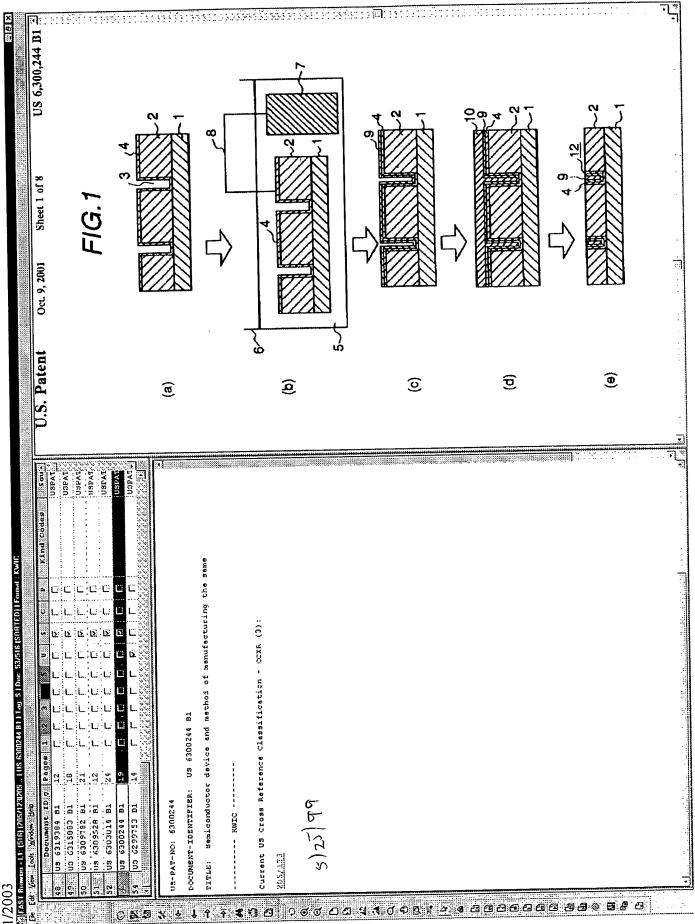
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semiconductor via by using forward and reverse pubes during the electroplating process which have time instrvals between pulses which lucrase with time and for forming conductive layers in semiconductor channels by using for ward pulses ching; the electroplating process which have time inservals between pulses which also increase with time. This elluys itsi deposition while reducing the deposition stress to eliminate voids and speeced up the overstil manufacturing process. Alar C. West, Chin-Chang Cheng, and Brett C. Baker, "Phise Reverse Capper Electrodeposition in High Aspect Ratio Treathers and Visa", J. Electrochemical Society, vol. 145, no. 5, pp. 3070–3074, 5p. 1998.

Yes' Stechau-Diamana & Sergey, Loyain, "High Aspect Ratio Quarter-Micros Electroless Coppet Integrated Technology", Microelectronic Engineering, 3708, 1997, pp. 2000gy", Microelectronic Engineering, 3708, 1997, pp. L.M. Weisenberger, "Copper Plating", Messis Handbook Ninh Edition, vol. 5: Surface Cleaning, Finishing, and Costing, American Society for Metals, pp. 159-169. A method is provided for forming conductive layers in 204,231 US 6,297,157 B1 Oct. 2, 2001 Primary Examiner—Charles Bowers Assistant Examine—Thanbts Phera (74) Anomey, Agent, or Firm—Mikio Ishinstra 20 Claims, 3 Drawing Sheets OTHER PUBLICATIONS 7/1994 Engelbaupi ..... 306C 306D 308 (10) Patent No.: (45) Date of Patent: 306B \( \) cited by examiner 5,326,454 3040 304C 3048 304 Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days. 204/15 204/14.1 428/635 204/58.5 TIME RAMPED METHOD FOR PLATING OF HIGH ASPECT BATIO SEMICONDUCTOR VIAS AND CHANNELS Sergey D. Lopath, Santa Clare, Matthew S. Buynoski, Paio Alto, both of CA (US) Advanced Micro Devices, Inc., Suanyvale, CA (US) (12) United States Patent U.S. PATENT DOCUMENTS 302D 302C References Cited 41998 Rac et al. ... 51987 Loch ....... 91989 Nee et al. ... 81991 Mullarkey . 302 302B Nov. 1, 1999 Appl. No.: 09/431,516 Lopath et al. Field of Scarch aventors: Assignee: 4.214,265 4,606,567 4,669,971 5,639,381 Notice: Filed: – გ> 3 3 (31) (52) (58) ε (35) e ₹ 9 7 USPAT USPAT USPAT USPAT USPAT TITLE: Time temped method for plating of high aspect ratio semiconductor vias and chonnels corr Ш + L1: [516] (205/123/2005 .. | US 6297157 R1 | Tay S 1 Dive; 56/516 (SORTED) Current US Cross Reference Classification - CCXR (2): 3 о 0 us 6297157 B1 В 45 Document ID 9 DOCUMBNT-IDENTIFIER: US 6277260 B1 US-PAT-NO: 6297157 us 6284121 Bi ua 6297157 pl US 6299751 B1 118 6287443 B1 US 6277262 B1 NNHC 205/123 ତି**ଅଧେ**୪ ନ**ୀ । ୯୧ଣରେ | ୪୯୯ ସସ ଶସ୍ଧ୍ୟ ନ୍**ଞ ମସର**୍ବସନ୍ତ୍ର** 880

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